A LOW-CURRENT LINEARITY SWEET SPOT IN HFET'S

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ABSTRACT

Planar doped HFET's exhibit a narrow bias region of low intermodulation distortion, a linearity sweet spot, at low drain current levels. The bias condition associated with this sweet spot is shown to be near the low-current inflection point of the transconductance versus gate voltage characteristic. It is also shown that the bias condition for the sweet spot can be controlled in dual-gate HFET's. This feature in the HFET characteristics can be exploited to design low-power front-end MMIC's with better intercept points for applications in wireless communications.

I. INTRODUCTION

Wireless communication applications require circuits with the lowest possible dissipated power, but still with high gain, low noise figure and low distortion. HFET's, because of their well known advantage in gain and noise figure over MESFET's, are being used in increasing numbers in RF and microwave communication circuit designs [5]. The one area of reported disadvantage for HFET's is their linearity [6]. The trend in receiver front-end designs for wireless communications is toward lower device operating currents [1-5]. As HFET's are biased closer to pinch off in order to reduce their drain current, there is a general trend toward higher levels of intermodulation distortion. However, there is a narrow range of drain current near pinch-off, where the intermodulation distortion goes through a local minimum. This bias range will be referred to here as the low-current linearity sweet spot in the HFET characteristics.

II. DEVICE DATA

The devices tested were 600 μm wide single- and dual-gate AlGaAs/InGaAs/GaAs pseudomorphic HFET's with silicon planar doping in the AlGaAs layer. The wafers were fabricated using a 0.7 μm GaAs HFET MMIC process. This process employs epitaxial material with a superlattice buffer, Ni/Ge/Au ohmics, Ti/Al Schottky gate and two-level metal interconnects.

The measurements were made at 1 GHz using an internally developed on-wafer automated test system. Intermodulation distortion is a function of the nonlinearity of the device parameters and source and load terminations at the primary and the generated signal frequencies. Intermodulation characterization is usually done in a 50-ohm testing environment on amplifier stages, which include both input and output impedance matching networks. On-wafer characterization of the intermodulation characteristics of discrete devices over a wide range of bias conditions requires well-defined terminating conditions for all bias points tested. Optimal source and load impedance matching of the measured device at the fundamental and the important generated frequencies is a formidable task. Matching errors would introduce uncertainty in the data and could distort the results. Thus, in order to expedite the measurements and to simplify the interpretation of the measured intermodulation data, it was decided to test discrete devices terminated with the 50-ohm test system impedance. A similar approach was used for the characterization of the transconductance nonlinearity in MESFET's [7].

The metric used for intermodulation distortion was the third-order intercept point [6] at 1 GHz

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using two signal sources with a 25 kHz frequency separation. The intercept point was projected from measurements made at signal output levels just 20 dB above the spectrum analyzer's noise floor with a 10-Hz IF bandwidth. Because the output power obtained under unmatched conditions does not fairly represent the device's performance capability, the intercept point was expressed in terms of available rf power from the source (incident power). To differentiate from the intercept point expressed in terms of the input power, IIP3, and in terms of the output power, OIP3 or simply IP3, the intercept point expressed in terms of the available source power will be denoted here by AIP3. AIP3 and OIP3 are related by the transducer power gain, G_t:

$$AIP3 = OIP3 / G_t \qquad (1)$$

Figure 1 shows AIP3 vs. gate bias for a single-gate HFET. AIP3 has a broad main peak for small positive gate voltages and a narrow secondary peak, the sweet spot, close to pinch off. Figures 2 and 3 show the dc drain current and the extrinsic transconductance, g_m, and its first and second derivatives with respect to the dc gate voltage, g_m' and g_m''. Extrinsic g_m includes the effects of the device parasitic resistance. The transconductance and its derivatives were obtained from measured 1 GHz s-parameters. The noise in g_m'' is due to s-parameter measurement errors.

III. OBSERVATIONS

Comparison of figures 1 and 3 reveals that the sweet spot is very nearly at the same bias as the transconductance inflection point, where g_m' is at a local maximum and $g_m'' = 0$. The conclusion must be that g_m'' is the dominant g_m distortion mechanism in AIP3 with the device near pinch off and terminated by 50 ohms at input and output. Note that the current in the area of the broad g_m peak is nearly 10 times higher than at the inflection point.

AIP3 for a FET with 50-ohm terminations can be estimated using [8]

$$AIP3\ (dBm) = 10 \log \left| 60\, g_{mi}(1 + g_{mi} r_s)^2 / [g_{mi}'' - 3 (g_{mi}')^2 r_s]/(1 - g_{mi} r_s) \right| \qquad (2)$$

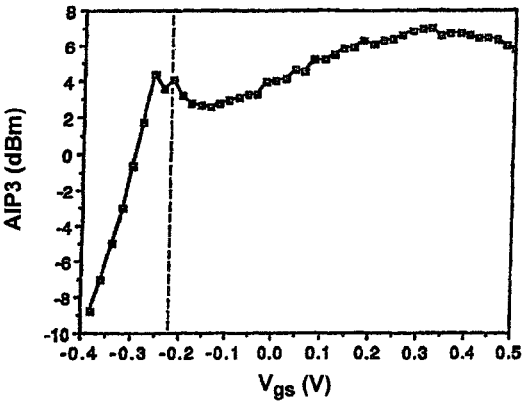

Figure 1. Measured AIP3 of a single-gate HFET.

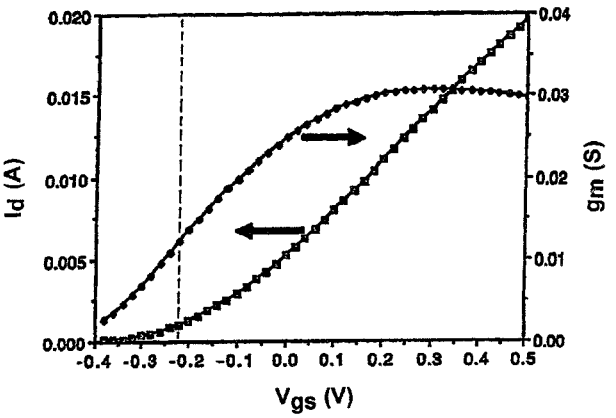

Figure 2. Dc drain current and 1 GHz extrinsic transconductance.

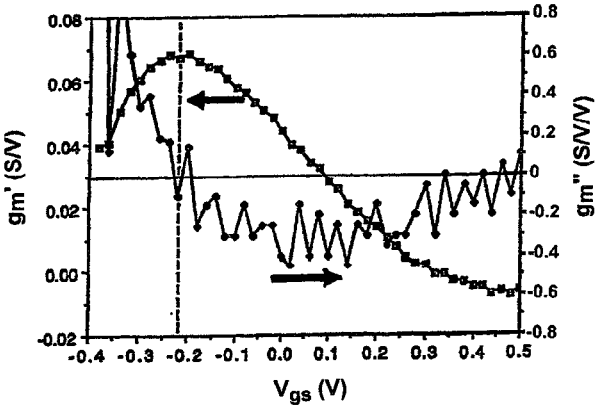

Figure 3. First and second derivatives of 1 GHz extrinsic transconductance.

where g_{mi}, g_{mi}', and g_{mi}'' refer to the *intrinsic* transconductance and its derivatives and r_s is the parasitic device source resistance. The same expression in terms of the *extrinsic* transconductance can be obtained by setting $r_s = 0$:

$$\text{AIP3 (dBm)} = 10 \log |60\ g_m/g_m''| \qquad (3)$$

Estimation of AIP3 using (3) compares well with the shape and the magnitude of the measured AIP3 as shown in figure 4. A more accurate comparison requires a smoother estimate of g_m''.

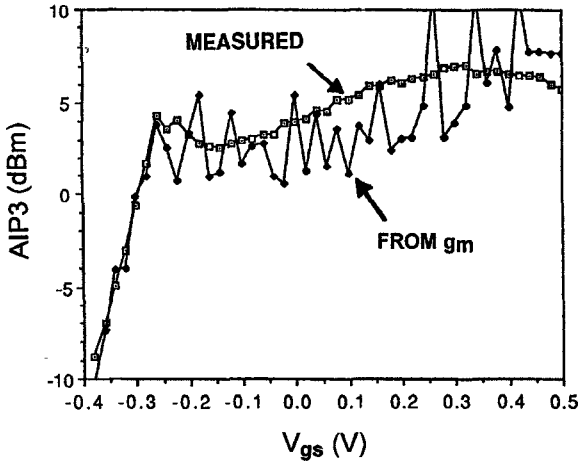

Figure 4. AIP3 directly measured and calculated from 1 GHz extrinsic transconductance.

It is interesting to note that equation (3) does not include g_m'. This is because equation (2) was derived by assuming that transconductance is the dominant nonlinearity and that the other parameter nonlinearities can be neglected. A more detailed derivation [9], including the nonlinearities of input capacitance, C_g, and output conductance, g_o, reveals that g_m' *does* contribute to IP3 by way of products

$$g_m' g_o' \quad \text{and} \quad g_m' C_g',$$

where g_o' is the first derivative of g_o with respect to the drain voltage and C_g' is the first derivative of C_g with respect to the gate voltage. Thus, expression (3) is useful for locating the linearity sweet spot and for estimating AIP3 for most values of gate voltage, but it cannot predict the value of AIP3 at the singular bias condition where $g_m'' = 0$.

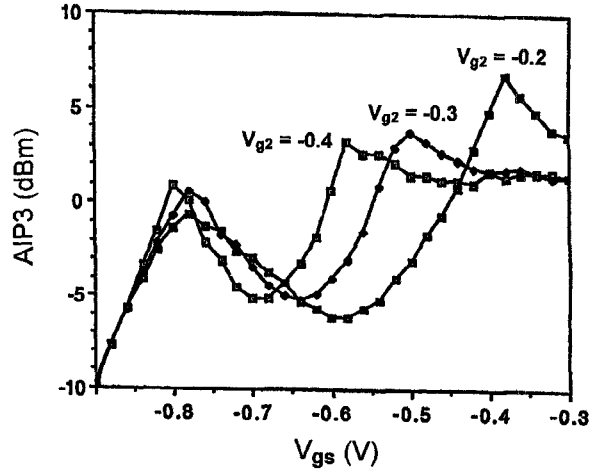

Figure 5. Second gate bias control of AIP3 in a dual-gate HFET.

Figure 5 shows a plot of AIP3 for a dual-gate HFET for 3 different values of the second gate voltage. It demonstrates that the second gate bias voltage affects the location of the low-current linearity sweet spot and the shape of the AIP3 characteristic. Thus, the second gate bias voltage can be used to adjust or control the linearity of dual-gate HFET amplifiers.

IV. CONCLUSIONS

A linearity sweet spot was identified for HFET's operating at low current levels. The extrinsic g_m was obtained from 1 GHz s-parameters and was used to estimate the third-order intercept point of HFET's. The estimated AIP3 was found to approximate the projected values of AIP3 measured using two rf signals with closely spaced frequencies centered at 1 GHz. The bias condition associated with the linearity sweet spot was shown to be near $g_m'' = 0$, the low-current inflection point of the g_m versus gate voltage characteristic. It was also shown that the bias condition for the sweet spot can be controlled in dual-gate HFET's.

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